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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,221	10/08/2003	Tatsuro Yamazaki	021910.000093	4174

5514 7590 08/02/2006

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EXAMINER	
LIANG, REGINA	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 08/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/680,221	**Applicant(s)** YAMAZAKI ET AL.	
	Examiner Regina Liang	**Art Unit** 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.
  4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) 1-12 is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  a)☒ All b)☐ Some * c)☐ None of:
    1.☒ Certified copies of the priority documents have been received.
    2.☐ Certified copies of the priority documents have been received in Application No. _____.
    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
  * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
  Paper No(s)/Mail Date 9/20/05, 4/18/05, 11/18/03, 10/30/03, 10/8/03.
4) ☐ Interview Summary (PTO-413)
  Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 1-8, 12, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 1, the phases "wherein the scanning circuit is one which applies the scanning signals to a part and the plurality of scan interconnections out of the plurality of scan interconnections in one select period" is confusing since it is not understood what is the plurality of scan interconnections out of the plurality of scan interconnections. The phases "wherein the output from the scanning circuit has a low level portion in which signal level is controlled to low level between said scanning signals which are applied repeatedly to scanning interconnection" is also confusing since it is not understood what is meant by a low level portion and low level between the scanning signals.

Claims 5, 7, 12 are unclear for depending from "any one of claims 1".

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Kuo (US 5,742,270).

FIG. 1 of Kuo teaches a display device comprising a plurality of display device; a plurality of scanning lines and a plurality of data lines, a canning circuit (33) for outputting scanning signals sequentially with scanning the plurality of scanning lines. Kuo also teaches the display device having a control circuit for controlling the scanning circuit in accordance with one scanning condition of a plurality scanning conditions (the display device having different scanning methods, see Figs. 5-7), such as the number of scanning lines to which are selected simultaneously in each select period (one scanning method as shown in Figs. 6A, 6B), or number of the scanning lines to which the scanning signals are applied repeatedly in successive two select period (another scanning method as shown in Fig. 7A), a modulation circuit (data driver) for applying a modulation signal to the modulation lines, and the control circuit for controlling the scanning conditions as claimed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuo in view of Aratani (US 6,100,872 hereinafter Aratani).

Kuo teaches the display device having a plurality of scanning conditions (note the discussion of claim 9 above). Kuo does not disclose the control circuit changing the scanning conditions based on the input signal from a signal input terminal. However, Aratani teaches a display device having an interlacing scanning and non-interlacing scanning, a control circuit changing the scanning conditions based on the input signal from a signal input terminal (col. 7, lines 49-53 for example). Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the control circuit of Kuo to have the teachings as taught by Aratani as a result of which a flicker-free image having a high picture quality can be displayed at high speed (col. 2, lines 15-23 of Aratani).

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kabayashi in view of Saito et al (US 6,366,026 hereinafter Saito).

As to claim 11, Fig. 2 of Kabayashi discloses an image display apparatus, comprising a plurality of display device, a plurality of scan lines and a plurality of modulation lines (signal lines), a scanning circuit (60) for applying scanning signals to the scanning lines, a modulation circuit (70) for applying a modulation signal to the modulation lines (signal lines). Fig. 3 and 5 of Kabayashi teaches the scanning circuit applies the scanning signals to a plurality of adjacent scanning lines in one select period and applies the scanning signals to a plurality of scan lines which were shifted with one scan line from the plurality of scanning line to which the scanning signals were applied in a previous select period, in a subsequent select period.

Kabayashi does not disclose the modulation circuit applying a pulse width modulation signal to the signal line and apply one pulse width modulation signal in one select period. However, Figs. 4 and 5 of Saito teaches a display device comprising modulation circuit (column driver 22, 23), the column driver applies a pulse width modulation signal to the column signal line, and applies one pulse width modulation signal in one select period. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the modulation circuit of Kabayashi to apply pulse width modulation signal to the signal line as taught by Saito so as to provide a display device with gray-scale control.

7. Claims 1, 5, 6, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kabayashi et al (EP 0 272 079 hereinafter Kabayashi) in view of Yamazaki (US 7,030,851).

As to claim 1, Fig. 2 of Kabayashi discloses an image display apparatus, comprising a plurality of display device, a plurality of scan lines and a plurality of modulation lines (signal lines), a scanning circuit (60) for applying scanning signals to the scanning lines, a modulation circuit (70) for applying a modulation signal to the modulation lines. Figs. 3 and 5 of Kabayashi teaches the scanning circuit applies scanning signals to a plurality of scanning lines in one select period, and applies the scanning signals in a subsequent select period, to the plurality of scanning lines which were shifted with one scan line from a group of scanning lines to which the scanning signals were applied in a pervious select period, and applies the scanning signals to the scanning lines in successive two select periods.

Kabayashi does not disclose the output of the scanning circuit has a low level signal. However, Yamazaki teaches an output signal of the scanning circuit is controlled by a pulse signal DY of each vertical scanning period, such as low level signals as selecting signals are outputted from the scanning circuit if the pulse signal DY has a low level signal (see Fig. 4 for example, the selecting signals for scanning lines Y1-Ym have low level signal when DY has low level signal). Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the scanning signal of Kabayashi to have low level as selected signals as taught by Yamazaki so as to control and supply scanning signals to the scanning lines.

As to claim 5, Fig. 3 of Kabayashi teaches applying scanning signals with different potentials to a plurality of scanning lines which are selected in one select period (Ts).

As to claim 6, Fig. 6 of Kabayashi teaches a scanning signal having the highest level (5V0) in each of successive select periods to a different scanning line.

As to claim 12, Fig. 3 of Kabayashi teaches potential difference between the scanning signal and data signal.

8. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kabayashi and Yamazaki as applied to claim 1 above, and further in view Kuo.

As to claims 2, 3, Kabayashi as modified by Yamazaki does not disclose the display apparatus having a first scanning condition and a second scanning condition.

However, Kuo teaches a display device having different scanning conditions (different scanning methods, see Figs. 5-7), in a first scanning condition, the scanning signals are applied in a successive select period to a predetermined number of scanning lines which were shifted with one scanning lines from the a plurality of scanning lines to which the scanning signals were applied in a previous select period (Figs. 7A, 7B); in a second scanning condition the number of scanning lines to which the scanning signals are applied simultaneously in one select period (Figs. 6A, 6B). Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the display apparatus of Kabayashi as modified by Yamazaki to have a first scanning condition and a second scanning condition as taught by Kuo so that the brightness difference in pixels caused by cell capacitance is eliminated (col. 2, lines 37-38 of Kuo).

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kabayashi, Yamazaki, Kuo as applied to claim 2 above, and further in view of Aratani.

Kabayashi as modified by Yamazaki and Kuo does not disclose the control circuit changing the scanning conditions based on the input signal from a signal input terminal. However, Aratani teaches a display device having an interlacing scanning and non-interlacing scanning, a control circuit changing the scanning conditions based on the input signal from a signal input terminal (col. 7, lines 49-53 for example). Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the control circuit of Kabayashi as modified by Yamazaki and Kuo to have the teachings as taught by Aratani as a result of which a flicker-free image having a high picture quality can be displayed at high speed (col. 2, lines 15-23 of Aratani).

10. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kabayashi and Yamazaki as applied to claim 1 above, and further in view Someya et al (US 6,924,796 hereinafter Someya).

As to claim 7, Kabayashi as modified by Yamazaki does not disclose the display apparatus comprising a correction circuit for emphasizing an edge of an image which is displayed. However, Someya teaches a display device comprising a correction circuit (4-6 in Fig. 6) for correcting the dot clock frequency of the input signal and for emphasizing an edge of an image which is displayed (col. 4, line 66 to col. 5, line 6, col. 5, lines 54-66). Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the display apparatus of Kabayashi as modified by Yamazaki to have a correction circuit as taught by Someya for providing edge enhancement and improving the displayed image quality.

As to claim 8, Someya teaches the correction circuit is configured to select level of correction (col. 6, lines 1-55).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (571) 272-7693. The examiner can normally be reached on Monday-Friday from 8AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Regina Liang
Primary Examiner
Art Unit 2674

7/28/06